

Listing of Claims:

Entire set of pending claims:

203. (Canceled)

1 204. (New) An apparatus comprising:
2 a host interface in an optical drive controller, said host interface operable to be
3 directly connected to a host computer via an IDE/ATA bus to
4 communicate addresses, commands, and data through ATA command
5 block register addresses, said host interface including a first buffer
6 addressed by one said ATA command block register addresses and
7 operable to store command packets, each of said command packets
8 comprising multiple command bytes received through multiple writes by
9 said host computer as part of a single command transfer and stored
10 sequentially in said first buffer, wherein said first buffer provides a greater
11 amount of storage than the width of said IDE/ATA bus.

1 205. (New) The apparatus of claim 204, wherein said host interface is further operable
2 to provide access by a microcontroller to data stored in locations addressed by at least
3 certain of said ATA command block register addresses, said microcontroller operable to
4 control reading of information from optical media.

1 206. (New) The apparatus of claim 204, wherein said optical drive controller further
2 comprises:

3 a path operable to communicate said addresses and commands from the host
4 interface to a microcontroller, said microcontroller operable to control
5 reading of information from optical media.

1 207. The apparatus of claim 206 wherein said microcontroller is also operable to cause
2 the assertion of signals on DASP and PDIAG lines of said IDE/ATA bus.

1 208. The apparatus of claim 206, wherein said microcontroller is also operable to cause
2 the assertion of signals on an HIRQ line of said IDE/ATA bus to generate interrupts on
3 said host computer.

1 209. The apparatus of claim 206, wherein:
2 said host interface includes a status register addressed by another of said ATA
3 command block register addresses, said status register including a BSY bit
4 whose state indicates whether said host computer can access said ATA
5 command block register addresses; and
6 said microcontroller can cause said BSY bit to be altered to a state that allows
7 access by said host computer.

1 210. (New) The apparatus of claim 204, wherein said ATA command block register
2 addresses address eight register locations.

1 211. (New) The apparatus of claim 204, wherein said IDE/ATA bus includes,
2 host address lines; and
3 a host chip select line whose signal identifies whether signals on the host address
4 lines are carrying one of said ATA command block register addresses.

- 1 212. (New) The apparatus of claim 204, wherein host interface includes physical
2 registers that are addressed by at least certain of said ATA command block register
3 addresses.
- 1 213. (New) The apparatus of claim 204, wherein said host interface supports all of the
2 signals required by the ATA transfer protocol.
- 1 214. (New) The apparatus of claim 204, wherein said IDE/ATA bus is at least 16 bits
2 wide.
- 1 215. (New) The apparatus of claim 204, wherein the one of said ATA command block
2 register addresses that can be used to address said first buffer is the address of a data port
3 in the ATA transfer protocol.
- 1 216. (New) The apparatus of claim 204, wherein said host interface also includes a
2 second buffer operable to store data to be transmitted to said host computer and addressed
3 by the one of said ATA command block register addresses that can be used to address
4 said first buffer.
- 1 217. (New) The apparatus of claim 216, wherein said second buffer is a queue or FIFO.
- 1 218. (New) The apparatus of claim 204, wherein said first buffer is a queue or FIFO.
- 1 219. (New) The apparatus of claim 204, wherein said optical drive controller further
2 comprises:
3 a path operable to allow a microcontroller, which controls reading of information
4 from optical media, to read said first buffer.

1 220. (New) The apparatus of claim 204, wherein said host interface includes a status
2 register addressed by another of said ATA command block register addresses, said status
3 register including a BSY bit.

1 221. (New) The apparatus of claim 220, wherein said host interface alters said BSY bit
2 when necessary to indicate when said host computer is precluded from accessing said
3 ATA command block register addresses.

1 222. (New) The apparatus of claim 220, wherein said host interface includes circuitry
2 operable to clear the signal on an HIRQ line of said IDE/ATA bus responsive to said host
3 computer reading said status register.

1 223. (New) The apparatus of claim 220, wherein said host interface includes circuitry
2 operable to alter said BSY bit, responsive to command events initiated by the host
3 computer, to a state that precludes said host computer from accessing said ATA
4 command block register addresses.

1 224. (New) The apparatus of claim 223, wherein said optical drive controller further
2 comprises:
3 a path operable to allow a microcontroller, which controls reading of information
4 from optical media, to alter said BSY bit to a state that allows said host
5 computer to access said ATA command block register addresses.

1 225. (New) The apparatus of claim 220, wherein said host interface is operable to
2 assert signals on DASP and PDIAG lines of said IDE/ATA bus according to the ATA
3 transfer protocol.

1 226. (New) The apparatus of claim 225, wherein said host interface is also operable to
2 assert signals on an HIRQ line of said IDE/ATA bus according to the ATA transfer
3 protocol.

1 227. (New) The apparatus of claim 226, wherein said host interface includes circuitry
2 operable to carry out initial signal transitions on said DASP, PDIAG, and HIRQ lines in
3 response to soft reset and execute drive diagnostic command events.

1 228. (New) The apparatus of claim 227, wherein said optical drive controller further
2 comprises:
3 a path operable to allow a microcontroller, which controls reading of information
4 from optical media, to control certain transitions of signals on said DASP,
5 PDIAG, and HIRQ lines of said IDE/ATA bus.

1 229. (New) The apparatus of claim 220, wherein said host interface is also operable to
2 assert signals on DASP and PDIAG lines of said IDE/ATA bus responsive to power on
3 reset or execute diagnostic commands received from said host computer.

1 230. (New) The apparatus of claim 229, wherein said optical drive controller further
2 comprises:
3 a path operable to allow a microcontroller, which controls reading of information
4 from optical media, to cause the assertion of signals on DASP and PDIAG
5 lines of said IDE/ATA bus.

1 231. (New) The apparatus of claim 204, wherein said host interface includes a
2 drive/head register addressed by another of said ATA command block register addresses,
3 said drive/head register including a DRV bit.

1 232. (New) The apparatus of claim 231, wherein said host interface uses said DRV bit
2 to determine whether to store command information in said first buffer.

1 233. (New) The apparatus of claim 204, wherein said host interface is also operable to
2 communicate control signals on at least certain control lines of said IDE/ATA bus.

1 234. (New) The apparatus of claim 233, wherein said control lines include HIRQ,
2 DASP, and PDIAG.

1 235. (New) The apparatus of claim 204, wherein said host interface is also operable to
2 assert signals on an HIRQ line of said IDE/ATA bus according to the ATA transfer
3 protocol.

1 236. (New) The apparatus of claim 204, wherein said host interface is also operable to
2 assert signals on an HIRQ line of said IDE/ATA bus to alert said host computer during
3 data transfers.

1 237. (New) The apparatus of claim 204, wherein said host interface is also operable to
2 assert signals on an HIRQ line of said IDE/ATA bus to allow said host computer to
3 engage in multi-tasking.

1 238. (New) An apparatus comprising:

2 a host interface of an optical drive controller, said host interface operable to be
3 directly connected to a host computer via an IDE/ATA bus to
4 communicate addresses, commands, and data through ATA command
5 block register addresses, said ATA command block register addresses
6 belonging to a register address map specified by an IDE/ATA bus
7 protocol, at least one of said ATA command block register addresses
8 providing access to a multi-byte command packet buffer that can store
9 multiple writes by the host computer of command information as part of
10 the same command and that provides a greater amount of storage than the
11 width of said IDE/ATA bus.

1 239. (New) The apparatus of claim 238, wherein said host interface is further operable
2 to provide access by a microcontroller to data stored in locations addressed by at least
3 certain of said ATA command block register addresses, said microcontroller operable to
4 control reading of information from optical media.

1 240. (New) The apparatus of claim 238, wherein said optical drive controller further
2 comprises:
3 a path operable to communicate said addresses and commands from the host
4 interface to a microcontroller, said microcontroller operable to control
5 reading of information from optical media.

1 241. The apparatus of claim 240, wherein said microcontroller is also operable to cause
2 the assertion of signals on DASP and PDIAG lines of said IDE/ATA bus.

1 242. The apparatus of claim 240, wherein said microcontroller is also operable to cause
2 the assertion of signals on an HIRQ line of said IDE/ATA bus to generate interrupts on
3 said host computer.

1 243. The apparatus of claim 240, wherein:
2 said host interface includes a status register addressed by another of said ATA
3 command block register addresses, said status register including a BSY bit
4 whose state indicates whether said host computer can access said ATA
5 command block register addresses; and
6 said microcontroller can cause said BSY bit to be altered to a state that allows
7 access by said host computer.

1 244. (New) The apparatus of claim 238, wherein said ATA command block register
2 addresses address eight register locations.

1 245. (New) The apparatus of claim 238, wherein said IDE/ATA bus includes,
2 host address lines; and
3 a host chip select line whose signal identifies whether signals on the host address
4 lines are carrying one of said ATA command block register addresses.

1 246. (New) The apparatus of claim 238, wherein host interface includes physical
2 registers that are addressed by at least certain of said ATA command block register
3 addresses.

1 247. (New) The apparatus of claim 238, wherein said host interface supports all of the
2 signals required by the ATA transfer protocol.

1 248. (New) The apparatus of claim 238, wherein said IDE/ATA bus is at least 16 bits
2 wide.

1 249. (New) The apparatus of claim 238, wherein the one of said ATA command block
2 register addresses that can be used to address said multi-byte command packet buffer is
3 the address of a data port in the ATA transfer protocol.

1 250. (New) The apparatus of claim 238, wherein said host interface also includes a
2 multi-byte data buffer operable to store data to be transmitted to said host computer and
3 addressed by the one of said ATA command block register addresses that can be used to
4 address said multi-byte command packet buffer.

1 251. (New) The apparatus of claim 250, wherein said multi-byte data buffer is a queue
2 or FIFO.

1 252. (New) The apparatus of claim 238, wherein said multi-byte command packet
2 buffer is a queue or FIFO.

1 253. (New) The apparatus of claim 238, wherein said optical drive controller further
2 comprises:
3 a path operable to allow a microcontroller, which controls reading of information
4 from optical media, to read said multi-byte command packet buffer.

1 254. (New) The apparatus of claim 238, wherein said host interface includes a status
2 register addressed by another of said ATA command block register addresses, said status
3 register including a BSY bit.

1 255. (New) The apparatus of claim 254, wherein said host interface alters said BSY bit
2 when necessary to indicate when said host computer is precluded from accessing said
3 ATA command block register addresses.

1 256. (New) The apparatus of claim 254, wherein said host interface includes circuitry
2 operable to clear the signal on an HIRQ line of said IDE/ATA bus responsive to said host
3 computer reading said status register.

1 257. (New) The apparatus of claim 254, wherein said host interface includes circuitry
2 operable to alter said BSY bit, responsive to command events initiated by the host
3 computer, to a state that precludes said host computer from accessing said ATA
4 command block register addresses.

1 258. (New) The apparatus of claim 257, wherein said optical drive controller further
2 comprises:
3 a path operable to allow a microcontroller, which controls reading of information
4 from optical media, to alter said BSY bit to a state that allows said host
5 computer to access said ATA command block register addresses.

1 259. (New) The apparatus of claim 257, wherein said host interface is operable to
2 assert signals on DASP and PDIAG lines of said IDE/ATA bus according to the ATA
3 transfer protocol.

1 260. (New) The apparatus of claim 259, wherein said host interface is also operable to
2 assert signals on an HIRQ line of said IDE/ATA bus according to the ATA transfer
3 protocol.

1 261. (New) The apparatus of claim 260, wherein said host interface includes circuitry
2 operable to carry out initial signal transitions on said DASP, PDIAG, and HIRQ lines in
3 response to soft reset and execute drive diagnostic command events.

1 262. (New) The apparatus of claim 261, wherein said optical drive controller further
2 comprises:
3 a path operable to allow a microcontroller, which controls reading of information
4 from optical media, to control certain transitions of signals on said DASP,
5 PDIAG, and HIRQ lines of said IDE/ATA bus.

1 263. (New) The apparatus of claim 254, wherein said host interface is also operable to
2 assert signals on DASP and PDIAG lines of said IDE/ATA bus responsive to power on
3 reset or execute diagnostic commands received from said host computer.

1 264. (New) The apparatus of claim 263, wherein said optical drive controller further
2 comprises:
3 a path operable to allow a microcontroller, which controls reading of information
4 from optical media, to cause the assertion of signals on DASP and PDIAG
5 lines of said IDE/ATA bus.

1 265. (New) The apparatus of claim 238, wherein said host interface includes a
2 drive/head register addressed by another of said ATA command block register addresses,
3 said drive/head register including a DRV bit.

1 266. (New) The apparatus of claim 265, wherein said host interface uses said DRV bit
2 to determine whether to store command information in said multi-byte command packet
3 buffer.

1 267. (New) The apparatus of claim 238, wherein said host interface is also operable to
2 communicate control signals on at least certain control lines of said IDE/ATA bus.

1 268. (New) The apparatus of claim 267, wherein said control lines include HIRQ,
2 DASP, and PDIAG.

1 269. (New) The apparatus of claim 238, wherein said host interface is also operable to
2 assert signals on an HIRQ line of said IDE/ATA bus according to the ATA transfer
3 protocol.

1 270. (New) The apparatus of claim 238, wherein said host interface is also operable to
2 assert signals on an HIRQ line of said IDE/ATA bus to alert said host computer during
3 data transfers.

1 271. (New) The apparatus of claim 238, wherein said host interface is also operable to
2 assert signals on an HIRQ line of said IDE/ATA bus to allow said host computer to
3 engage in multi-tasking.